Remarks/Argument

In the Office Action dated June 26, 2006, the Examiner rejected claims 1-5, 7-15, 17-25, 27-30, 36-38, 40-42, and 44-46 under 35 U.S.C § 103(a) as being unpatentable over Parks et al. ("Parks") (U.S. Patent No. 5,432,735). In addition, the Examiner allowed claims 31-35 and objected to claims 6, 16, 26, 39, 43, and 47, but indicated that claims 6, 16, 26, 39, 43, and 47 would be allowable if rewritten in independent form.

Applicant thanks the Examiner for the allowance of claims 31-35. By this Reply, Applicant has cancelled independent claims 1, 11, 21, 36, 40, and 44. In addition, Applicant has amended dependent claims 2, 12, 22, 37, 41, and 45 by rewriting them in independent form without changing the original scope of the claims. Applicant has also amended claims 3, 4, 5, 7, 9, 13, 14, 15, 17, 19, 23, 24, 25, 27, and 29 so that they properly depend from their respective base claims. Furthermore, in accordance with the Examiner's suggestion, Applicant has rewritten dependent claims 6, 16, 26, 39, 43, and 47 in independent form without changing the original scope of the claims. Claims 2-10, 12-20, 22-35, 37-39, 41-43, and 45-47 remain pending in this application.

Section 103(a) rejections

Applicant respectfully traverses the Section 103(a) rejections of claims 1-5, 7-15, 17-25, 27-30, 36-38, 40-42, and 44-46 as being unpatentable over Parks because Parks fails to disclose each and every claim element and the claim element(s) not disclosed by Parks would not be obvious to one having ordinary skill in the art. For example, claim 2 discloses a combination of elements including, *inter alia*, "M first terminals and N second terminals, where M and N are positive integers, and where $M > N > 1$ . . . wherein the N terminals are pin terminals." Parks fails to disclose at least these claim elements. Furthermore, Applicant submits that at least these claim elements are not known to one having ordinary skill in the art.

In the Office Action, the Examiner maintained that "limitations regarding a specific/further application (i.e., connections to a memory) [are] common practice in the art of IC interconnection[.]" Applicants respectfully draw the Examiner' attention to M.P.E.P § 2141 which states the standard of patentability to be applied in obviousness rejections. Specifically, M.P.E.P § 2141 states that:

> "[The] four factual inquires enunciated therein as a background for determining obviousness are as follows: (A) Determining the scope and contents of the prior art; (B) Ascertaining the differences between the prior art and the claims in issue; (C) Resolving the level of ordinary skill in the pertinent art; and (D) Evaluating evidence of secondary considerations." M.P.E.P § 2141 (I) (8th ed. Rev. 3, August 2005).

In addition, M.P.E.P. § 2141.02 clearly states that in ascertaining the differences between the prior art and the claims at issue, the claimed invention as a whole should be considered. Specifically, M.P.E.P. § 2141.02 states the following:

> "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." M.P.E.P § 2141.02 (8th ed. Rev. 3, August 2005).

Applicant respectfully submits that the claim elements of claim 2 are distinct from the teachings of Parks. For example, Parks discloses DRAM wherein each DRAM memory cell stores three states. See Parks, Abstract. Specifically, the apparatus in Parks includes a binary to ternary encoder 220 which converts binary bits into ternary data values. See Parks, column 3 line 35 to column 4 line 45. Furthermore, the DRAM in Parks store voltages based

on the ternary data values. See Parks column 4 lines 25 -45. That is, the memory cells in Parks have three possible states based on the ternary data values obtained from the binary to ternary decoder. In addition, during read operations, the ternary to binary decoder converts the ternary data stored in the memory cells back into binary data that is output to an external circuit. See Parks column 5, lines 35-45. See also, Parks FIG.2. Thus, it is abundantly clear that Parks discloses a ternary storage dynamic RAM wherein binary data is converted into ternary form so that it may be stored in the DRAM. Furthermore, this ternary data stored in the DRAM is converted back into binary form in order to be read by an external circuit.

Clearly, this teaching of Parks is distinct from at least the element of claim 2 which includes "wherein the N terminals are pin terminals." Specifically, claim 2 discloses that the data output from the integrated circuit of claim 2 is in ternary form. This is distinct from Parks which discloses that data output from the DRAM is in binary form. As described above, the main purpose of Parks is to store three states in a memory by using a combination of a binary to ternary encoder and a ternary to binary decoder. However, the data output from the DRAM to an external circuit in Parks is in binary form. This is distinct from the teachings of claim 2 wherein binary data is converted into ternary form in order to be output from an integrated circuit. In an attempt to used Parks as a Section 103(a) reference, the Examiner is arbitrarily reversing the set up in Parks which would defeat the purpose of the invention in Parks. Furthermore, in doing so, the Examiner has failed to consider the invention of claim 2 as a whole as required by the M.P.E.P. In addition, the Official Notice taken by the Examiner regarding the applicability of the encoder/decoder (see Office Action page 3, paragraph c) fails to remedy the deficiency of Parks. Therefore, for at least for the reason that all the elements of claim 2 are not disclosed, the Section 103(a) rejection of claim 2 should be withdrawn.

Claims 12, 22, 37, 41, and 45 are other independent claims that include features similar to those of claim 1. For example, claim 12 also

discloses a combination of elements including, *inter alia*, "N first terminals and M second terminals, where M and N are positive integers, and where M > N > 1 . . . wherein the N terminals are pin terminals." As discussed above, the combination of Parks and the Official Notice taken by the Examiner fails to disclose at least these claim elements. Likewise, claim 37 is a method claim including a combination of steps including, *inter alia*, "outputting the N base-K-level output signals to N output terminals of the integrated circuit device, respectively, wherein M, N, A and K are positive integers, wherein M > N > 1, wherein K > A > 1, and wherein the N output terminals are pin terminals of the integrated circuit device." As described above, the combination of Parks and the Official Notice taken by the Examiner fail to disclose at least these claim steps.

Dependent claims 3-5, 7-10, 13-15, 17-20, 23-25, 27-30, 38, 42, and 46 ultimately depend from one of claims 2, 6, 12, 16, 22, 26, 37, 39, 41, 43, and 45 and, therefore, are allowable for at least the reasons discussed above and in view of their additional recitations of novelty.

Claim objections

As mentioned above, in accordance with the Examiner's suggestion, Applicant has rewritten claims 6, 16, 26, 39, 43, and 47 in independent form without changing the original scope of the claims. Therefore, Applicant respectfully requests that the objection to claims 6, 16, 26, 39, 43, and 47 be withdrawn and these claims be allowed.

Conclusion

No other issues remaining, reconsideration and favorable action upon the claims 2-10, 12-20, 22-35, 37-39, 41-43, and 45-47 now pending in the application are requested.

Respectfully submitted,

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